

# A Comparative Study of Single Phase Grid Connected Phase Locked Loop Algorithms

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## Abstract

A Phase-Locked Loop (PLL) is a vital part of power inverters for achieving synchronization with the utility grid. Throughout the phase angle of the grid voltage, a reference signal is generated in order to synchronize the operation condition of the renewable energy generation systems with the utility grid. The present paper presents a comparative study of the enhancement for conventional phase-locked loop using four different filters, including adaptive notch filter, second order adaptive notch filter, generalized integrator filter and second order generalized integrator filter. A comparison among these four studied improvements was conducted under normal operation condition. On the other hand, the performance of these filters was tested under two abnormal scenarios; voltage sag and phase jump. The results showed that the second order generalized integrator based PLL has superior performance over the other filters based PLL under both normal and fault operation conditions. In contrast, the adaptive notch based filter based PLL has the lowest response under both operation conditions.

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**Keywords:** Phase-Locked Loop; Adaptive Notch filter; Generalized Integrator; SOGI; enhanced Phase-Locked Loop.

## 1. Introduction

Worldwide, electric power systems have experienced a rapid change due to the integration of new technologies, such as photovoltaic, wind generation and/or fuel cells generation systems. These comprehensive transformations into new generation technologies became a result of the depletion in the conventional fossil fuel resources, increasing the concerns regarding the environment. Power electronics have been used to interface these generation technologies with the conventional power system [1]. However, this interface creates inevitable new challenges for efficient and reliable operating and controlling the utility power grid.

For grid-connected inverters, phase angle is a vital piece of information for an accurate and efficient synchronization. Thus, a phase-locked technique is required to achieve this synchronization. In this research, a specific type of phase-locked loop technology is studied based on four different filter structures. Then, the performance of the four studied filters based Phase-Locked Loop (PLL) is compared under normal and fault operation conditions.

Voltage source inverters enable the new generation technologies to be utilized as a dynamic voltage regulator through dynamic controlling of the voltage at the point of common coupling. However, they have more controlled variables compared with the conventional generation

technologies [2]. The fundamental phase angle of the utility voltage, for example, is a critical controlled variable for the grid synchronization. This angle is used to generate a reference signal in order to synchronize the operation condition of the distributed generation systems with the utility grid. As a result, an accurate phase tracking method is needed to achieve the phase angle information of the grid. Various phase tracking methods were developed which can be classified into two approaches. These are an open loop tracking approach (such as low pass filters, Kalman method, and space vector method) and a closed loop approach, such as a Phase-Locked Loop (PLL) [3].

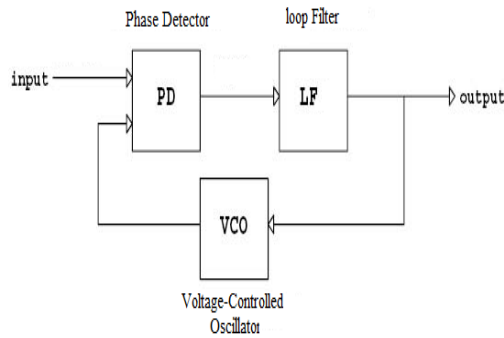
The PLL approach has been widely used in different systems, such as communication, motor control and other industrial applications. In power system fields, this technique has been adopted to provide fast and accurate synchronization between the generation side and the utility [4, 5, 6]. It should have a high immunity to disturbances, such as harmonics, noises, sags, unbalances and other distortions.

The PLL technique can be divided according to its structure into Stationary Reference (SR) frame-based PLL, Synchronously Rotating Reference frame (SRF), or Zero Crossing Detection (ZCD)-based PLL. The ZCD-based PLL method is sensitive to frequency transient and distortion notch [7]. SR frame and SRF-based PLLs do not work accurately during unbalance condition [8, 9]. Thus, the Enhanced PLL (EPLL) has been adopted as it has a

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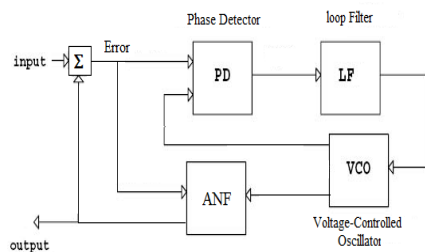
high degree of immunity to harmonic and unbalance conditions over conventional PLLs [5], [10, 11].

The operation principle of the conventional PLL is accomplished through a Phase Detector (PD), where the fundamental phase component is estimated [13]. Therefore, the output signal of the PD is filtered by a Loop Filter (LF) before entering a Voltage Controlled Oscillator (VCO), where it is synchronized with the input signal as shown in Figure (1)



**Figure 1.** Block diagram of a basic phase locked loop

An Adaptive Filter (AF) works on the concept of the Adaptive Noise Cancelling (ANC) concept, at which its own parameters are automatically adjusted. An Adaptive Notch Filter (ANF) technique is used in PLL to attenuate specific range of frequencies of the input signal to enhance the performance of the PD of the conventional PLL. Figure (2) illustrates the main concept of ANF where the output of the VOC is applied to the PD as a reference signal.

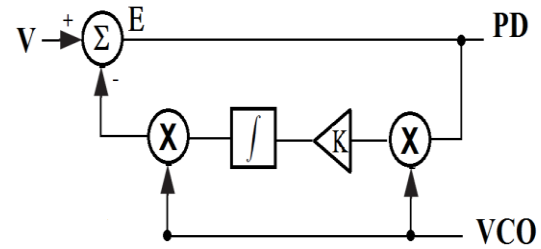


**Figure 2.** Block diagram of an enhanced phase locked loop with adaptive notch filter

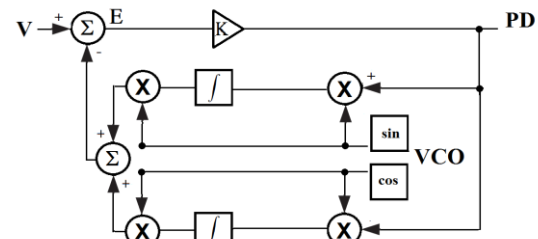
PD causes a phase shift by  $90^\circ$  between the input phase signal and the reference phase signal. Yet, ANF generates zero-signal for the PD as the PLL locked to the input signal. The design of a PLL can be optimized more by introducing a second order ANF which is built based on the ANC where the reference signal need to be filtered. However, the amplitude integrator in the second order ANF does not act ideally for the sinusoidal input signal with the center frequency of the VCO but depends on of the input signal, and its output contains a steady-state error [9].

In order to cancel this error, the Generalized Integrator (GI) adaptive filter is adopted. In this technique, the error is cancelled at a resonance frequency. However, as the GI based filter is a function of feed-forward frequency which restricts its applications in a variable-frequency environment. Thus, the Second Order Generalized Integrator based filter (SOGI) has been introduced as a good technique for variable frequency application, since it

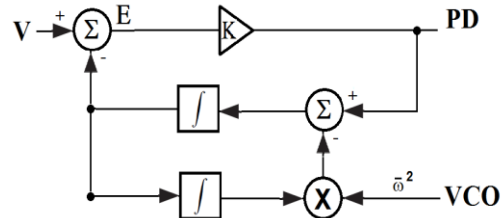
is a function of the gain only [14, 15]. Figure (3) shows the structure of the four studied filters.



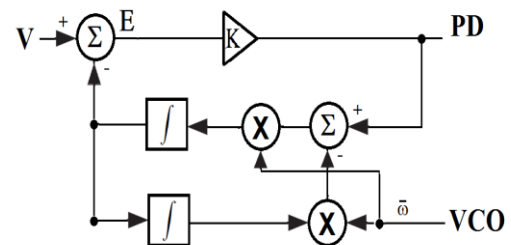
(a) first order adaptive notch filter



(b) second order adaptive notch filter



(c) generalized integrator filter



(d) second order generalized integrator filter

**Figure 3.** Structure of four filters based phase locked loop

The aim behind the present work is to design the phase-locked loop with conventional adaptive notch filter, second order adaptive notch filter, generalized integrator filter and second order generalized integrator. Then, the performance of the enhanced phase-locked loop algorithms are simulated and analyzed in the Matlab/Simulink computer environment under normal operation condition and then during fault scenarios

## 2. Methodology

The mathematical modeling of a PLL is adopted based on the system in [9- 11, 13], where the Phase Detector (PD) finds the difference between the input signal applied to the system and the output signal generated by VCO, which is known as the error. The output of PD has the double frequency ripple which can be partially removed using a loop filter. As a result, the LP bandwidth needs to

be small in order to remove the double frequency ripple and other distortions but not too small that affects the system response. Finally, the VCO changes its operating frequency when the error is not zero in order to generate the output signal at center frequency.

After the parameters of the design were calculated, the four studied PLLs were tested under a normal operation condition in Matlab environment. During normal operation condition, a single phase voltage 1 per unit was applied to the four filters based PLLs as an input with 50 Hz frequency, where the performance of the PLLs is compared. After that, a comparison of the PLLs is done under two fault scenarios: voltage sag and phase jump.

Voltage sag is defined as reductions in the grid voltage, lasting from a cycle to seconds, which are caused by unexpected increases in loads such as faults, or by sudden increases in source impedance. In this scenario, voltage amplitude of input signal is reduced by 70% from its value, during the second half of sample period, which gives a rise to high short circuit currents. Finally, during the phase jump scenario the phase is jump after one minute of simulation period.

The PLL can mathematically be interpreted as in equations (1), (2) and (3):

$$e(t) = V_{in}(t) - V_{out}(t) \quad (1)$$

$$V_{in}(t) = V \sin(\omega t - \varphi_{in}) \quad (2)$$

$$V_{out}(t) = V \sin(\omega t - \varphi_{out}) \quad (3)$$

where  $e(t)$  is the output signal of the PD, which is known as error signal,  $V_{in}(t)$ , is the input signal of EPLL, and  $V_{out}(t)$  is the output signal of the PLL. Clearly, that the error is a multivariable function of voltage magnitude, frequency and phase angle. As a result, this error cost function needs to be minimized in the sense of the linear least square, as shown in equation (4).

$$E(V, \omega, \varphi) = \|V_{in} - V_{out}\|^2 \quad (4)$$

By using the method of steepest descent, the following three differential equations can be obtained:

$$\dot{v}(t) = K e(t) \sin(\varphi_{out}) \quad (5)$$

$$\Delta \dot{\omega}(t) = K_i e(t) \cos(\varphi_{out}) \quad (6)$$

$$\dot{\varphi}_{out}(t) = (\omega_0 + \omega_{out}) K_p e(t) \cos(\varphi_{out}) \quad (7)$$

where  $K, K_i$ , and  $K_p$  are step size. By using linear analysis [12], equations (5), (6) and (7) can be expanded to:

$$\dot{V} \approx \frac{K}{2} (V_{in} - V_{out}) \quad (8)$$

$$\dot{\omega}(t) = \frac{K_i}{2} V_{in} (\varphi_{in} - \varphi_{out}) \quad (9)$$

$$\dot{\bar{\varphi}}(t) = (\omega_{out} - \omega_{in}) + \frac{K_p}{2} V_{in} (\varphi_{in} - \varphi_{out}) \quad (10)$$

where  $\bar{\omega} = \omega_{out} - \omega_{in}$  is the estimated angular frequency and  $\bar{\varphi} = \varphi_{out} - \varphi_{in}$  is the estimated phase. From these equations the approximated transfer function of the closed-loop system gives:

$$\frac{K_p V_{in}}{2} = 2\zeta\omega_n \quad (12)$$

$$\frac{K_i V_{in}}{2} = \omega_n^2 \quad (13)$$

$$K = \frac{2}{\tau} \quad (14)$$

The design parameters are shown in Table (1), where  $\zeta$  is damping ratio, which controls how fast the filter reaches its settle point and how much overshoot can have. In general, most of the control systems, except for robotic control systems, are designed with damping factor  $\zeta < 1$  to achieve a high response speed consistent [16]. Thus, damping factor  $\zeta = 0.7$  is chosen where, at this value, the system converges reasonably fast. Note that feed-forward frequency is;  $\omega_0 = 100\pi$  rad/s, at which the output of the regulator is zero once the regulator has tracked the phase.

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**Table 1.** Design Parameters

Parameters	Values
$\zeta$	0.7
$\tau$	2ms
$\omega_0$	314rad/s
K	500
K <sub>p</sub>	10,000
K <sub>i</sub>	200
F	50Hz

To do a comparison between control systems, two indices are considered: the integration for the square of the error (ISE) and the integration for the absolute magnitude of the error (IAE) are given by:

$$ISE = \int_0^{\infty} e(t)^2 dt \quad (15)$$

$$IAE = \int_0^{\infty} |e(t)| dt \quad (16)$$

where the system with the minimum indices is considered the best control system.

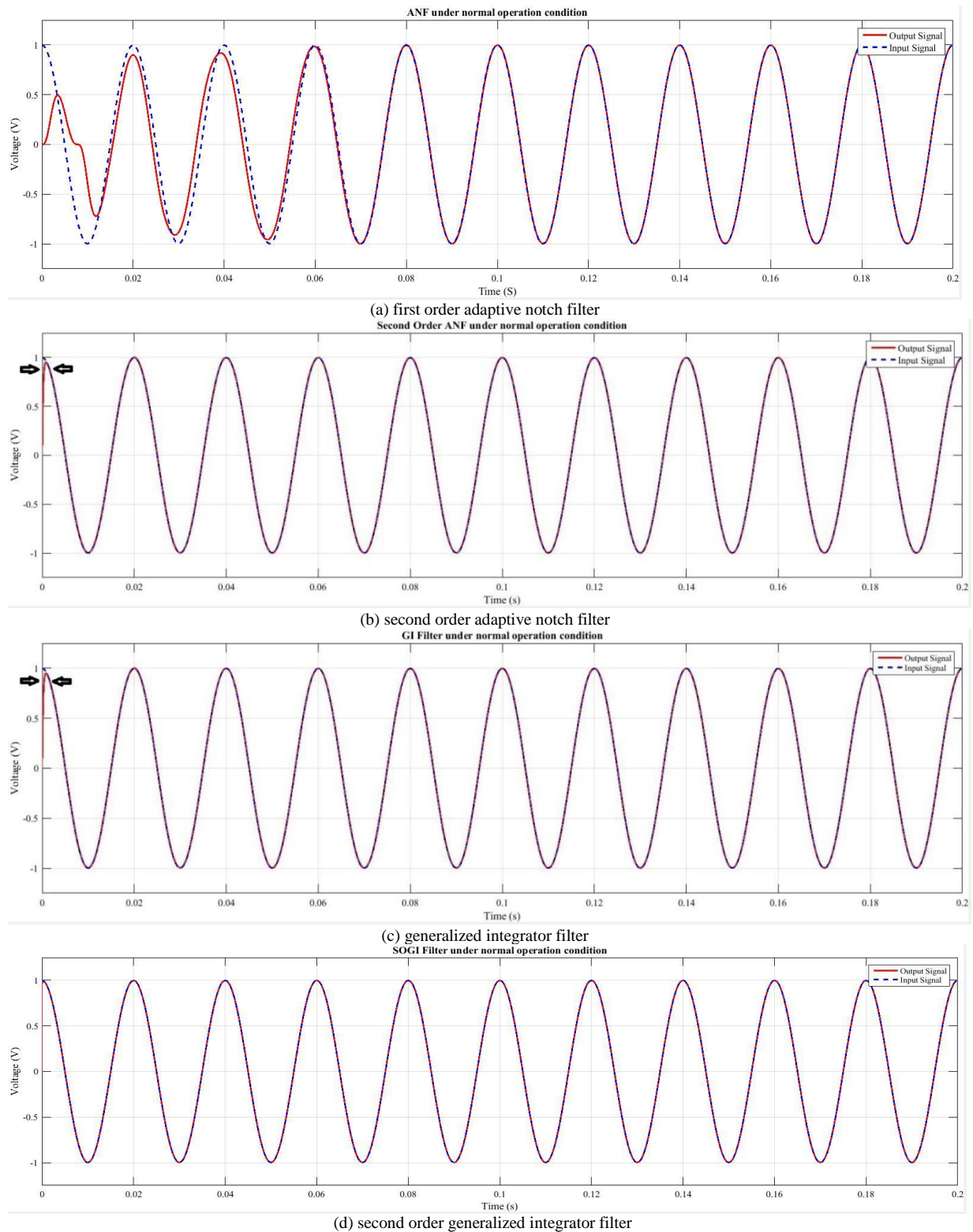
### 3. Results and Discussions

To test the performance of a fast and accurate synchronization of PLL, it has been simulated in MATLAB under normal and grid fault conditions. During different fault scenarios, the single phase voltage experience transients due to the appearance of voltage sags and frequency jump.

### 3.1. The PLL Response under Normal Operation Condition

The second order generalized integrator based PLL has the fastest and the most efficient response, as depicted in Figure (4-d), compared with other filters based PLLs. This result shows the ability of SOGI filter based PLL of

tracking the input signal without delay due to its resonance at the fundamental frequency [17]. GI-based PLL has the second best response, as illustrated in Figure (4-c), where it locked the reference signal during the first cycle. While the ANF-based PLL tracking the input signal, after about 70 ms, makes it the slowest tracking technique among the four filters.



**Figure 4.** the PLL response during normal operation condition

Moreover, Figure (5) illustrates the error signal of the four proposed techniques. Clearly, the SOGI filter-based PLL has zero error signal faster than the other three filter-based PLLs. In addition, the error signal of GI filter and second order ANF-based PLL have almost the same response. The amplitude integrator in the second order ANF and GI filter do not act ideally for the sinusoidal input signal, as mentioned [9]. Moreover, the error signal of SOGI filter-based PLL reaches zero steady state much faster than other filters.

The integration error values for the four filters based PLL are depicted in Table (2). It is obvious that SOGI filter-based PLL has the lowest ISE and IAE values, which indicates that SOGI has the best response, compared with the other three filters under normal operation condition. In comparison, ANF has the highest ISE and IAE, which shows that ANF-based PLL has the worst phase locking characteristics among the four proposed filters.

**Table 2:** The ISE and IAE for the Four Proposed Filters Based PLLs under Normal Operation Condition

Error Signal	ANF	Second Order ANF	GI Filter	SOGI Filter
ISE	5.602mV	99.68 $\mu$ V	99.72 $\mu$ V	3.175 $\mu$ V
IAE	14.22mV	0.4111mV	0.422mV	15.61 $\mu$ V

### 3.2. The PLL Response under Different Fault Conditions

Now, the performance of the four filters based PLL are simulated for two different fault scenarios. The following is a detailed presentation of these scenarios.

#### 3.2.1. Scenario 1: Voltage Sag

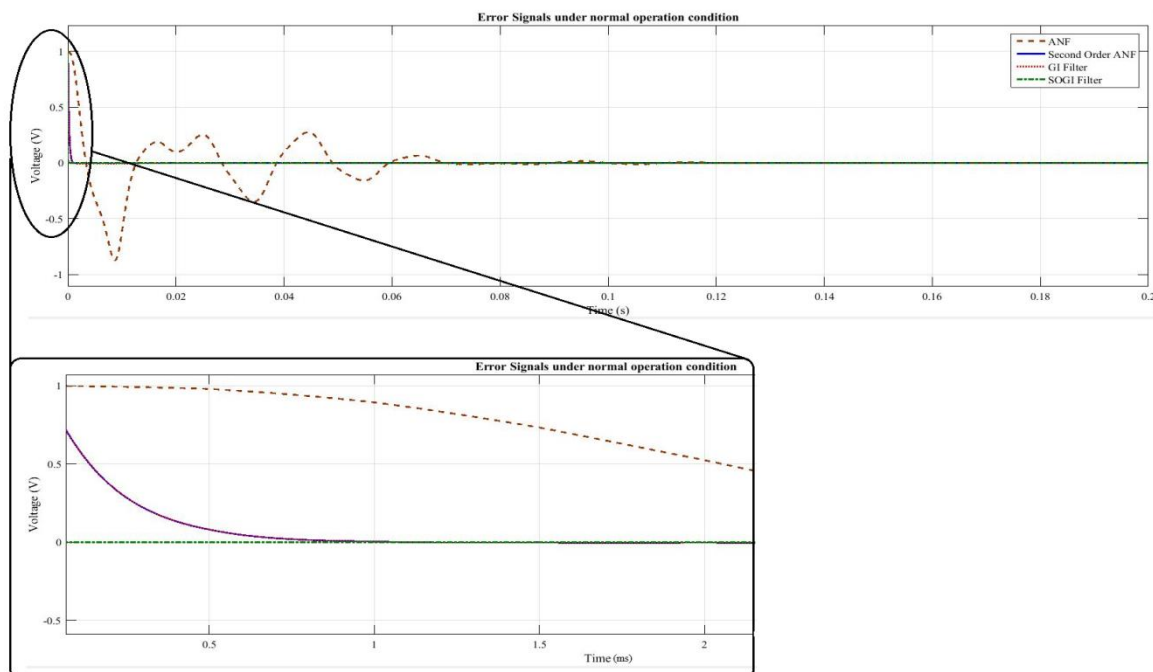
During this scenario, as depicted in Figure (6), the ANF-based PLL output signal was able to lock with the input signal after about two cycles from fault, despite of its ability for providing an output signal locked to the fundamental component of the input signal in its amplitude and frequency [3], while the SOGI-based PLL keeps tracking the input signal even during fault. In contrast, both second order ANF and GI filter-based PLL show acceptable level of immunity against voltage sag.

Further, Figure (7) depicts that once the SOGI-based PLL has the lowest zero error signal during fault condition, while the ANF-based PLL error signal experiences the oscillations after the fault occurs. This oscillation in error signal resulted experimentally in [18]. As its output, signal locked to the fundamental component of the input signal in its amplitude and frequency results in a high steady state error.

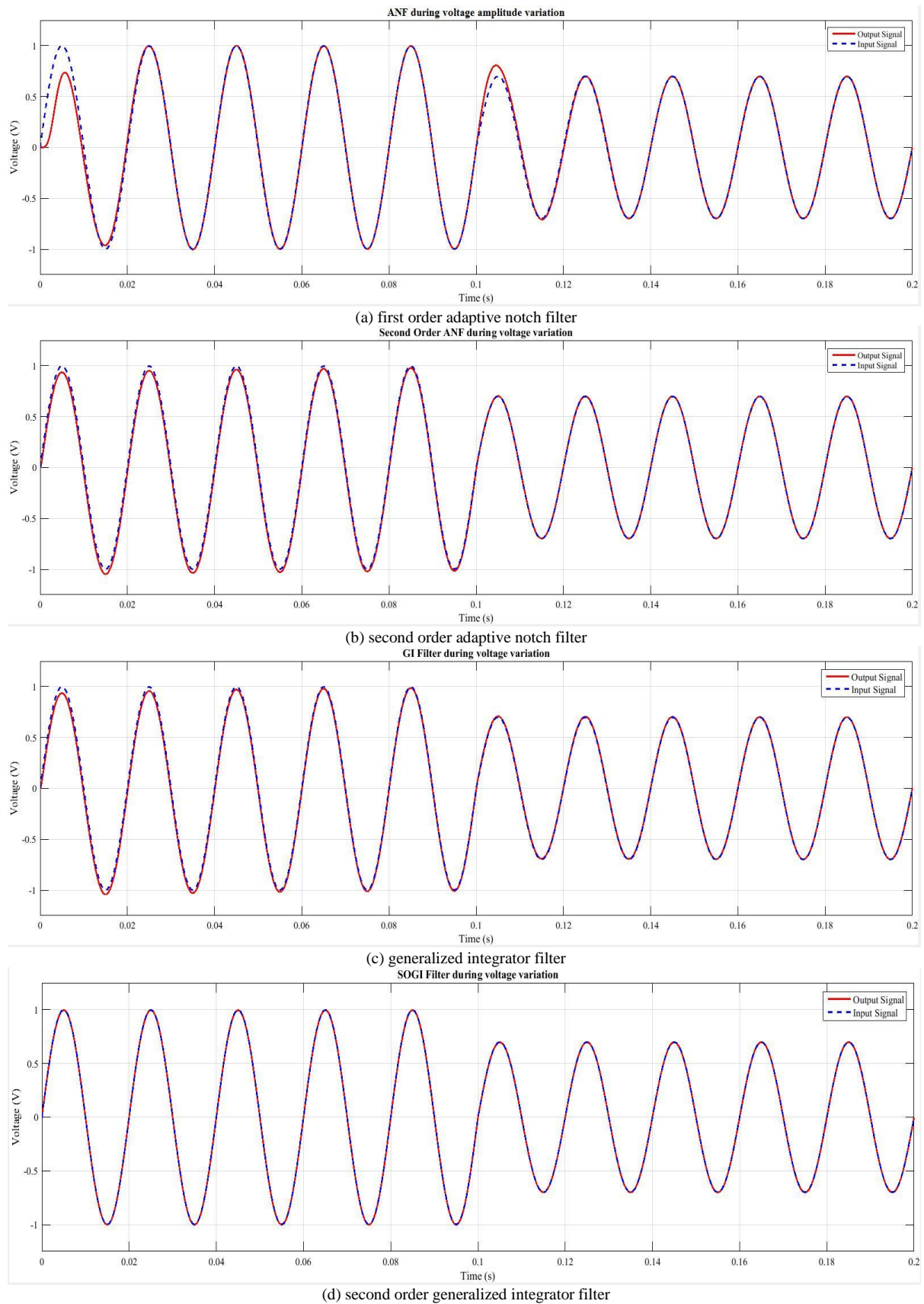
Clearly, the SOGI filter-based PLL has the lowest error indices among other filter-based PLLs, as shown in Table (3). In addition, the ANF-based PLL has the highest indices due to its operation principle as discussed before.

**Table 3:** The ISE and IAE for the Four Proposed Filters Based PLLs under Voltage

Error Signal	ANF	Second Order ANF	GI Filter	SOGI Filter
ISE	1.123mV	0.1379mV	0.1034mV	0.274 $\mu$ V
IAE	5.244mV	3.61mV	3.209mV	0.3172mV

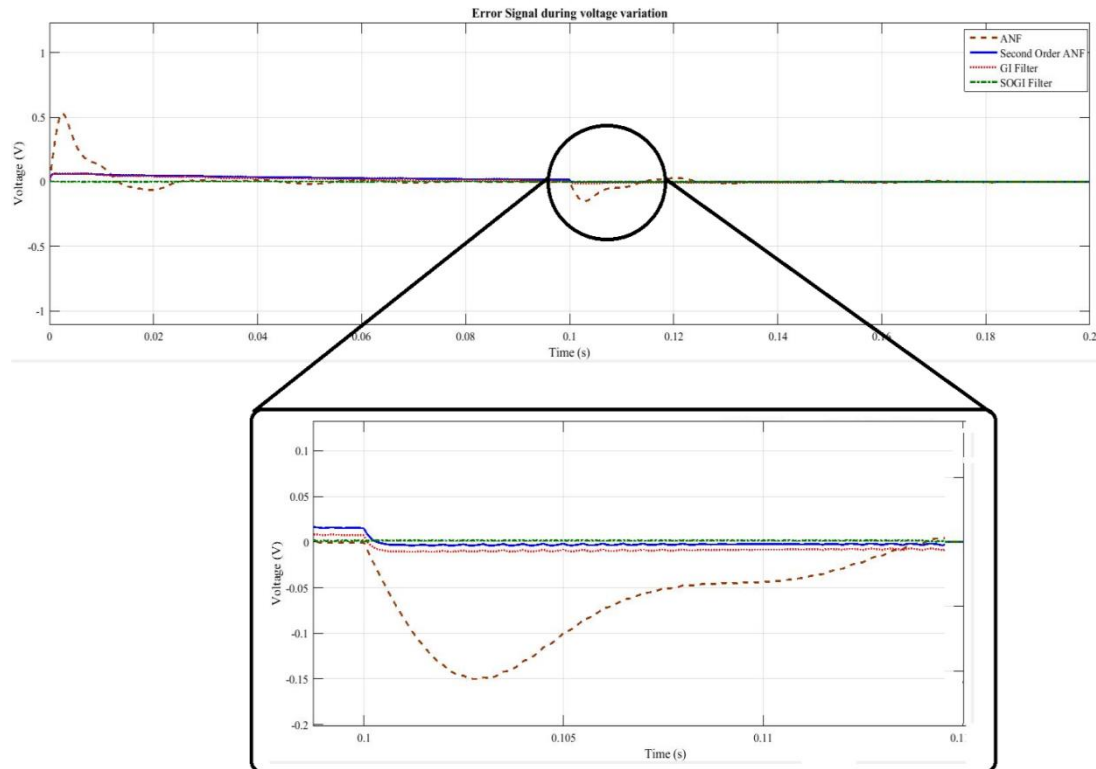


**Figure 5.** Error signal under normal operation condition



**Figure 6.** the PLL response during voltage sag





**Figure 7.** Error signal under voltage sag condition

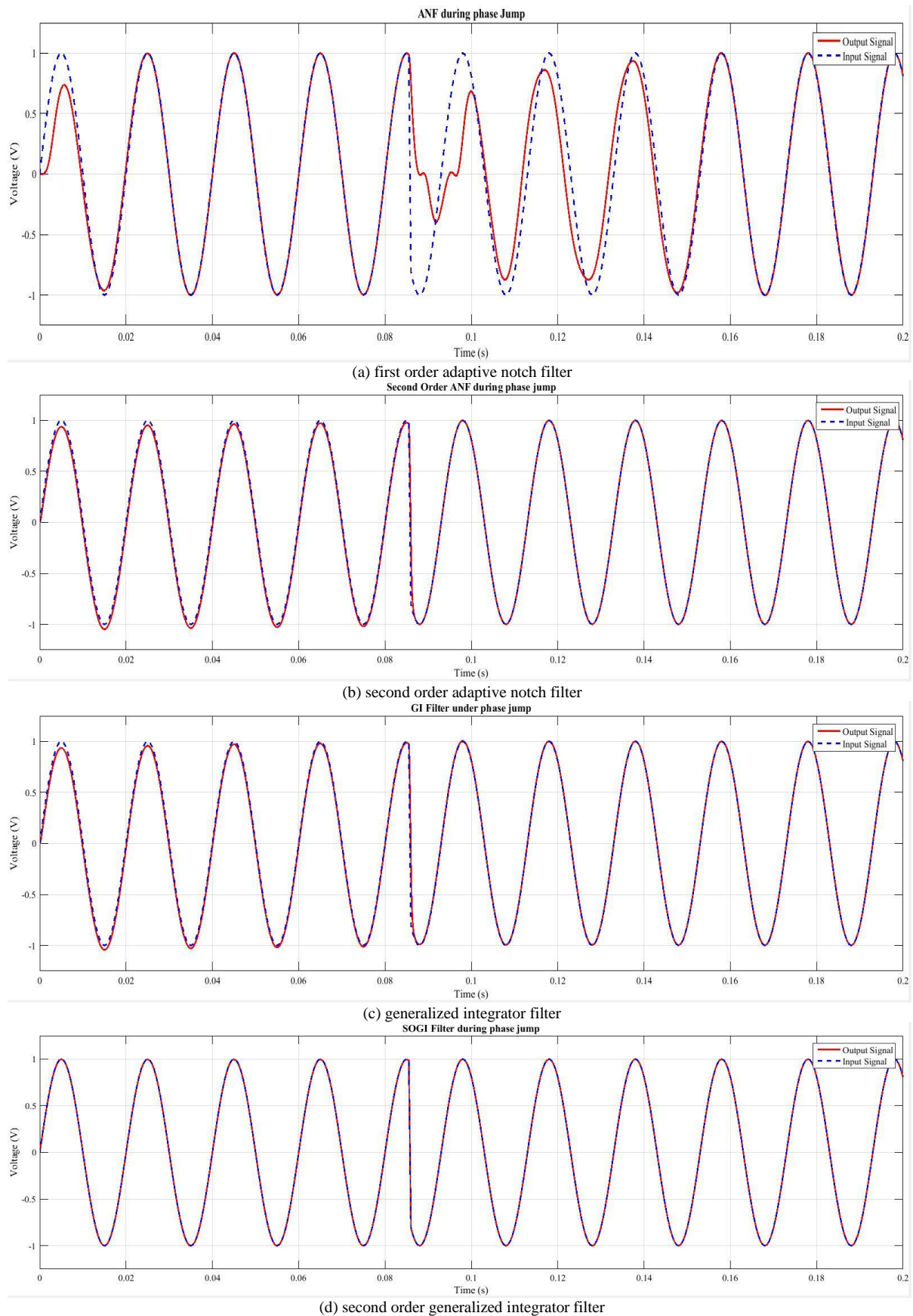
### 3.2.2. Scenario 2: Phase Jump

During this scenario, a phase jump occurs after about 86ms. As illustrated in Figure (8), the ANF-based PLL mistraces the input signal for about three cycles after the faults occur. This result shows that the ANF-based PLL is highly effected by phase jump, in comparison with the other three filters, which are able to keep locked with the input signal even after the phase jump take place. However, the SOGI-based PLL has the lowest error response during phase jump, as shown in Figure (9), while ANF-based PLL error signal experiences a high oscillation once the fault takes place. The same result was reported by [18] experimentally during phase. This severe response is attributed to the fact that ANF-based PLL output signal is locked to the fundamental component of the input signal in

its amplitude and frequency which reflects in a high oscillation error once any distortion affect the input signal. Finally, the errors of the proposed filter-based PLLs are also tested using ISE and IAE indices, as shown in Table (4). It is obvious that SOGI-based filter has the lowest ISE and IAE, while the ANF-based PLL has the highest ones.

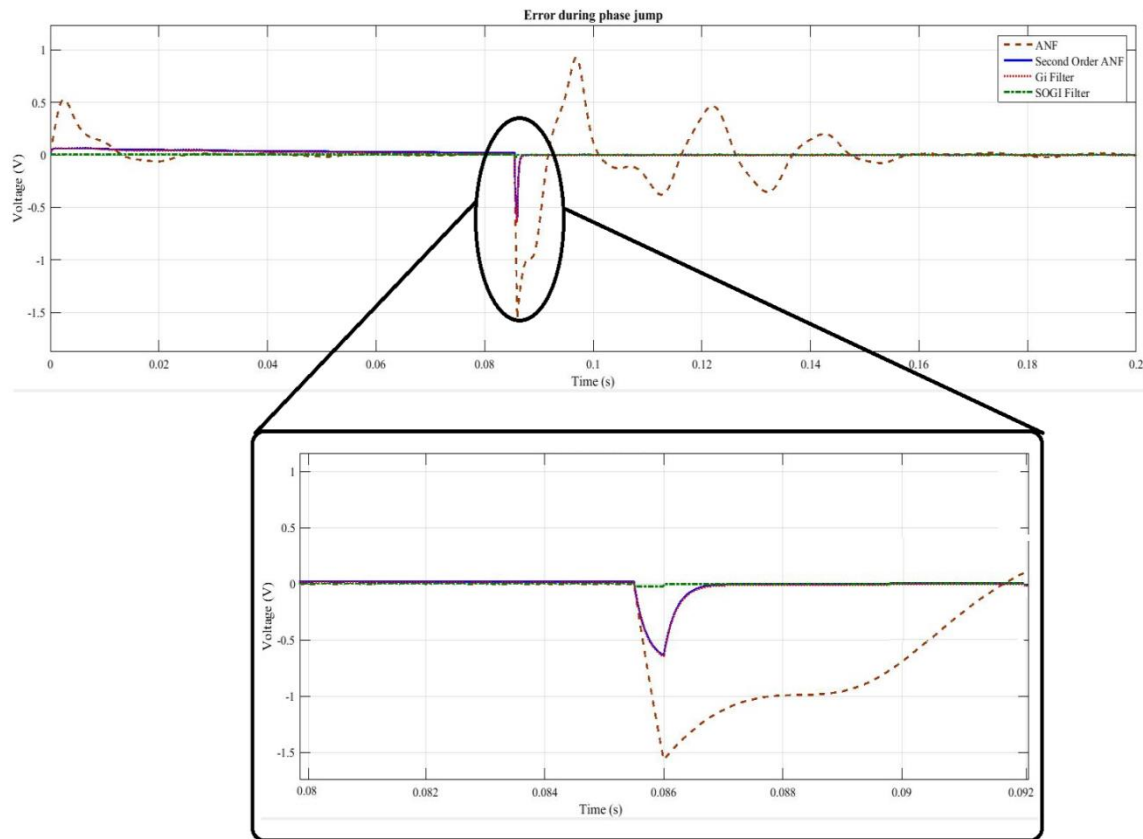
**Table 4:** The ISE and IAE for the four proposed filters based PLLs under phase jump condition

Error Signal	ANF	Second Order ANF	GI Filter	SOGI Filter
ISE	11.43mV	0.2834mV	0.2583mV	0.4411mV
IAE	23.23mV	3.598mV	3.321mV	0.2939mV



**Figure 8.** the PLL response during phase jump





**Figure 9.** Error signal under phase jump condition

#### 4. Conclusion

In order to achieve synchronization with the utility grid, a phase locked loop is used. It generates a reference signal to synchronize the operation condition of the inverter side with the utility grid. In the present study, an enhancement for a conventional phase locked loop using four different filters, including adaptive notch filter, second order adaptive notch filter, generalized integrator filter and second order generalized integrator filter, were investigated. Then a comparison between these four proposed improvements was conducted under normal and two abnormal operation condition scenarios: voltage sag and phase jump.

The results show that the second order generalized integrator based PLL has a superior performance over other filters-based PLL under both normal and fault operation conditions. During normal condition, the SOGI based PLL locked the input signal very fast and accurate. Moreover, it kept tracking the input signal even after the occurrence of a fault condition, such as a phase jump or voltage sag.

The ANF-based PLL had a sluggish response to reach zero steady state error signal during normal operation condition as well as during voltage sag. In addition, its error signal experienced a high oscillation during phase jump at which the output signal of this PLL missed the input signal and relock back again after three cycles.

In comparison with the second order ANF-based PLL, the GI-based PLL has a negligible enhancement over the former under both normal and abnormal operation condition.

In general, the four different filter techniques have an acceptable performance during the proposed operation conditions. The preferability of any of these filters-based PLL depends on its application in power system environment.

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